REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-14 are currently pending. Claims 1-14 have been amended by the present amendment. The changes to the claims are supported by the originally filed specification and do not add new matter.

In the outstanding Office Action, Claims 1-6 and 8-13 were rejected under 35 U.S.C. § 112, second paragraph regarding the phrase "or the like"; Claims 1-4, 6-11, 13, and 14 were rejected under 35 U.S.C. § 102(b) as being anticipated by Japanese Patent No. JP357125590 to Matsuda (hereinafter "the '590 patent"); and Claims 5 and 12 were indicated as allowable if rewritten to overcome the rejections under 35 U.S.C. § 112, second paragraph.

Applicants wish to thank the Examiner for the interview granted Applicants' representative on August 26, 2004, at which time the outstanding rejection of the claims was discussed. At the conclusion of the interview, the Examiner agreed that element 4 of the '590 patent is a clamping circuit, not an image writing unit, and that element 9 of the '590 patent is not configured to receive data from an image reading unit or an image processing unit. However, no formal agreement on the allowability of the claims was reached pending Examiner's further consideration of the claims upon formal submission of a response to the outstanding Office Action.

Applicants respectfully submit that the rejection of the claims under 35 U.S.C. § 112, second paragraph, is rendered moot by the present amendment to Claims 1 and 8. Claims 1 and 8 have been amended to delete the phrase "or the like."

Amended Claim 1 is directed to an image processor, comprising: (1) image memory configured to store image data; (2) an image memory control unit, which is connected to at least one connected unit, including at least one of an image reading unit for reading image

data, an image processing unit for processing and editing image data, and an image writing unit for writing image data to transfer paper, and is configured to receive at least one of first image data written by the image reading unit and second image data subjected to image processing by the image processing unit, to transmit at least one of the first image data and the second image data to the image memory, and to transmit the image data stored in the image memory to at least one of the image processing unit and the image writing unit; (3) a system control unit configured to control transmission or reception of control signals used in each of the connected units or between the connected units; (4) a source detection unit configured to detect a source of image data to the image memory control unit. Further, amended Claim 1 recites that the system control unit is configured to control the image memory control unit according to the source of the image data detected by the source detection unit, and to determine a transmission order of the image data to the image memory. In addition, Claim 1 has been amended to recite that the image memory control unit is configured to control access to the image memory so as to prevent a collision between jobs relating to accesses of the image memory, based on priorities of the jobs. No new matter has been added. As a non-limiting example, Figs. 2 and 4 show that the access control section 409 (image memory control unit) arbitrates access in order to avoid interference when the memory group 222 (image memory) is accessed by a plurality of units.

Regarding the rejection of Claim 1 as anticipated by the '590 patent, the '590 patent is directed to a still picture transmitter in which a still video image is divided into four parts for transmission on a low-speed transmission line. The '590 patent discloses that, in the transmitter, a video signal is compressed so that a screen size becomes ¼ of its original size and is stored in a memory specifying an address corresponding to screen position of upper-left, upper-right, lower-left, and lower-right. The compressed video signal is converted into a low-speed video signal and then transmitted. As shown in Figure 1, the '590 patent discloses

a switcher 1, a low-pass filter 2, a synchronizing signal separator 3, a clamping circuit 4, an A/D converter 5, a memory 8, a control circuit 6, a clock generator 7, and an address generator 9.

Initially, Applicants note that, contrary to the assertion in the Office Action, element 4 shown in Figure 1 of the '590 patent is a clamping circuit, not an image writing unit. Further, Applicants note that the Office Action has asserted that the address circuit/generator 9 reads on the image memory control unit recited in Claim 1. However, Applicants respectfully submit that the address generator 9 disclosed by the '590 patent is not configured to receive at least one of first image data written by the image reading unit and second image data subjected to image processing by the image processing unit, as recited in Claim 1. Rather, the address generator 9 is configured to send an address signal to the memory 8 to control the storage of video data in the memory 8. Thus, the '590 patent fails to disclose that the address generator 9 receives any image data at all. Further, Applicants respectfully submit that the address generator 9 disclosed by the '590 patent is not configured to transmit at least one of the first image data and the second image data to the image memory, as recited in amended Claim 1. The '590 patent fails to disclose that image data is transmitted from the address generator 9, but merely indicates that an address is sent from the address generator 9 to the memory 8. Further, Applicants respectfully submit that the address generator 9 disclosed by the '590 patent is not configured to transmit images stored in the image memory to at least one of the image processing unit and the image writing unit, as recited in amended Claim 1. The '590 patent fails to disclose that the address generator 9 transmits any image data whatsoever.

Moreover, Applicants note that the Office Action asserts that the synchronizing signal separator 3 reads on the claimed source detection unit recited in Claim 1. Further, Applicants note that Claim 1 recites that the source detection unit is configured to detect a source of

image data received by the image memory control unit. In contrast, Applicants respectfully submit that the synchronizing signal separator 3 disclosed by the '590 patent is configured to extract the synchronizing signal from the filtered video signal and to feed it to the clamping circuit 4.

Further, Applicants submit that the '590 patent discloses a correspondence between the memory area and the position on the original image before compression. However, Applicants respectfully submit that the '590 patent fails to disclose that the image memory control unit is configured to control access to the image memory so as to prevent a collision between jobs relating to accesses of the image memory, based on priorities of the jobs, as recited in amended Claim 1. Accordingly, for the reasons stated above, Applicants respectfully traverse the rejection of Claim 1 (and dependent Claims 2-4 and 6) as anticipated by the '590 patent.

Independent Claims 7, 8, and 14 recite limitations analogous to the limitations recited in Claim 1. Accordingly, for the reasons stated above for the patentability of Claim 1, Applicants respectfully traverse the rejection of Claims 7, 8, and 14 (and all associated dependent claims) as anticipated by the '590 patent.

Thus, it is respectfully submitted that independent Claims 1, 7, 8, and 14 (and all associated dependent claims) patentably define over the '590 patent.

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Consequently, in view of the present amendment and in light of the above discussion, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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